I²C-Compatible (2-wire) Serial EEPROM

2K/4K/8K/16K

DATASHEET

Features

- Compatible with all I²C bidirectional data transfer protocol
- Memory array:
  - 2K bits (256X 8)/ 4K bits (512 X 8) / 8K bits (1024 X 8) / 16K bits (2048 X 8) of EEPROM
  - Page size: 16 bytes
- Single supply voltage and high speed
  - 1 MHz
- Random and sequential Read modes
- Write:
  - Byte Write within 3 ms
  - Page Write within 3 ms
  - Partial Page Writes Allowed
- Write Protect Pin for Hardware Data Protection
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- High Reliability
  - Endurance: 1,000,000 Write Cycles
  - Data Retention: 100 Years
- Enhanced ESD/Latch-up protection
  - HBM 8000V
- 8-lead PDIP/SOP/TSSOP/UDFN and WLCSP4 packages

Description

- The ZD24C02A/ZD24C04A/ZD24C08A/ZD24C16A provides 2048/4096/8192/16384 bits of serial electrically erasable and programmable read- only memory (EEPROM), organized as 256/512/1024/2048 words of 8 bits each.

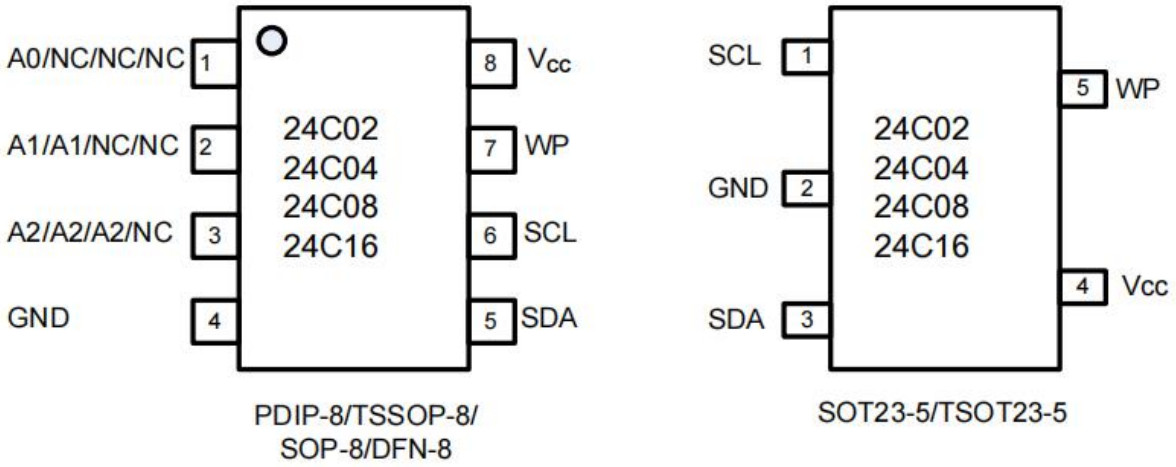
- The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential.

1. Pin Descriptions and Pinouts

Table 1-1.Pin Descriptions

Pin Number	Pin Symbol	Pin Name and Functional Description	Asserted State	Pin Type
1, 2，3	NC	**No Connect:** The NC pins are not bonded to a die pad. This pin can be connected to GND or left floating.	—	NC
1，2，3	A2 A1 A0	**Device Address Input:** The A2/A1/A0 pin is used to select the hardware device address . This pin can be directly connected to VCC or GND. Refer to Note 1 for behavior of the pin when not connected.	—	Input
4	GND	**Ground:** The ground reference for the power supply. GND should be connected to the system ground.	—	Power
5	SDA	**Serial Data:** The SDA pin is an open-drain bidirectional input/output pin used to serially transfer data to and from the device. The SDA pin must be pulled-high using an external pull-up resistor (not to exceed 10KΩ in value) and may be wire-ORed with any number of other open-drain or open-collector pins from other devices on the same bus.	—	Input/ Output
6	SCL	**Serial Clock:** The SCL pin is used to provide a clock to the device and to control the flow of data to and from the device. Command and input data present on the SDA pin is always latched in on the rising edge of SCL, while output data on the SDA pin is clocked out on the falling edge of SCL. The SCL pin must either be forced high when the serial bus is idle or pulled- high using an external pull-up resistor.	—	Input
7	WP	**Write Protect:** Connecting the WP pin to GND will ensure normal write operations. When the WP pin is connected to VCC, all write operations to the memory are inhibited. Refer to Note 1 for behavior of the pin when not connected.	High	Input
8	VCC	**Device Power Supply:** The V_{CC} pin is used to supply the source voltage to the device. Operations at invalid V_{CC} voltages may produce spurious results and should not be attempted.	—	Power

Note:1. If the A2/A1/A0 or WP pin is not driven, it is internally pulled down to GND. In order to operate in a wide variety of application environments, the pull-down mechanism is intentionally designed to be somewhat strong. Once these pins are biased above the CMOS input buffer's trip point (~0.5 x V_{CC}), the pull-down mechanism disengages. Zetta recommends connecting these pins to a known state whenever possible.



2. Device Block Diagram and System Configuration

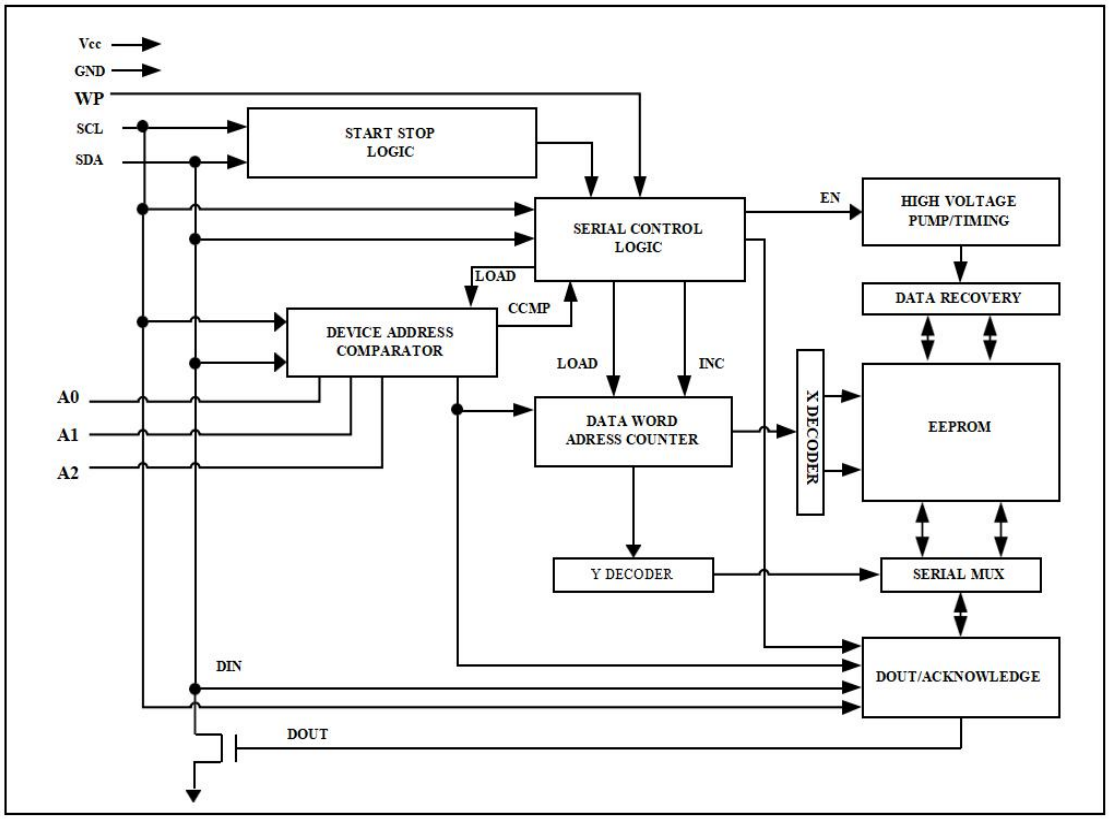


Figure 2-2.System Configuration Using 2-Wire Serial EEPROM

3. Device Operation and Communication

The ZD24C02A/ZD24C04A/ZD24C08A/ZD24C16A operates as a slave device and utilizes a simple I^2C-compatible 2-wire digital serial interface to communicate with a host controller, commonly referred to as the bus Master. The Master initiates and controls all read and write operations to the slave devices on the serial bus, and both the Master and the slave devices can transmit and receive data on the bus.

The serial interface is comprised of just two signal lines: Serial Clock (SCL) and Serial Data (SDA). The SCL pin is used to receive the clock signal from the Master, while the bidirectional SDA pin is used to receive command and data information from the Master, as well as, to send data back to the Master. Data is always latched into the ZD24C02A/ZD24C04A/ZD24C08A/ZD24C16A on the rising edge of SCL and always output from the device on the falling edge of SCL. Both the SCL and SDA pin incorporate integrated spike suppression filters and Schmitt Triggers to minimize the effects of input spikes and bus noise.

All command and data information is transferred with the Most-Significant Bit (MSB) first. During bus communication, one data bit is transmitted every clock cycle, and after eight bits (one byte) of data have been transferred, the receiving device must respond with either an Acknowledge (ACK) or a No-Acknowledge (NACK) response bit during a ninth clock cycle (ACK/NACK clock cycle) generated by the Master. Therefore, nine clock cycles are required for every one byte of data transferred. There are no unused clock cycles during any read or write operation, so there must not be any interruptions or breaks in the data stream during each data byte transfer and ACK or NACK clock cycle.

During data transfers, data on the SDA pin must only change while SCL is low, and the data must remain stable while SCL is high. If data on the SDA pin changes while SCL is high, then either a Start or a Stop condition will occur. Start and Stop conditions are used to initiate and end all serial bus communication between the Master and the slave devices. The number of data bytes transferred between a Start and a Stop condition is not limited and is determined by the Master. In order for the serial bus to be idle, both the SCL and SDA pins must be in the logic-high state at the same time.

3.1 Clock and Data Transition Requirements

The SDA pin is an open drain terminal and therefore must be pulled high with an external pull-up resistor. Data on the SDA pin may change only during SCL low time periods. Data changes during SCL high periods will indicate a Start or Stop condition as defined below.

3.2 Start and Stop Conditions

3.2.1 Start Condition

A Start condition occurs when there is a high-to-low transition on the SDA pin while the SCL pin is at a stable Logic 1 state and will bring the device out of standby mode. The Master uses a Start condition to initiate any data transfer sequence, therefore every command must begin with a Start condition. The device will continuously monitor the SDA and SCL pins for a Start condition but will not respond unless one is detected. Please refer to Figure 3-1 for more details.

3.2.2 Stop Condition

A Stop condition occurs when there is a low-to-high transition on the SDA pin while the SCL pin is stable in the Logic 1 state. The Master can use the Stop condition to end a data transfer sequence with the ZD24C02A/ZD24C04A/ZD24C08A/ZD24C16A which will subsequently return to standby mode. The Master can also utilize a repeated Start condition instead of a Stop condition to end the current data transfer if the Master will perform another operation. Please refer to Figure 3-1 for more details.

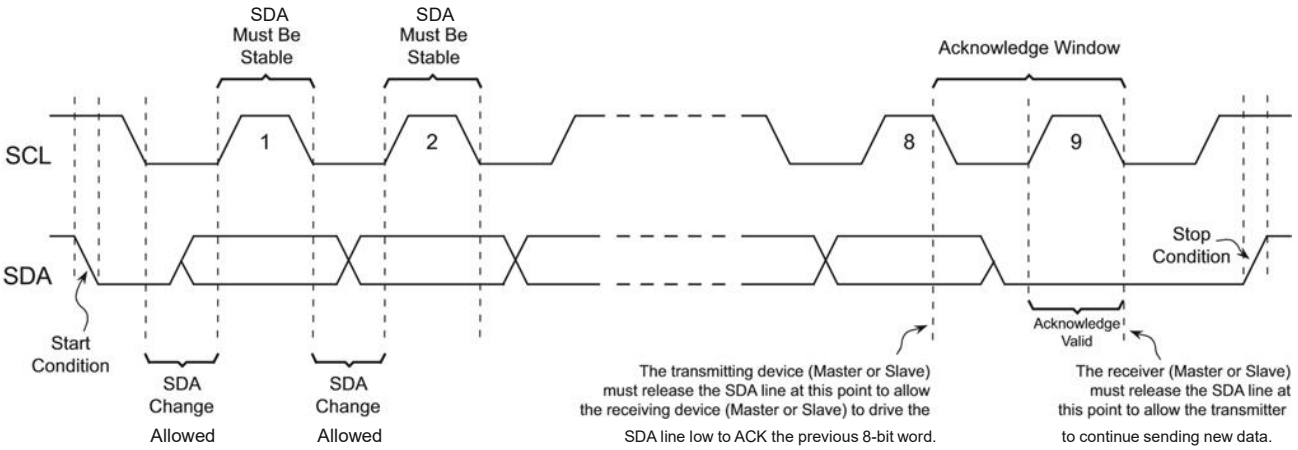
3.3 Acknowledge and No-Acknowledge

After every byte of data is received, the receiving device must confirm to the Master that it has successfully received the data byte by responding with what is known as an acknowledge (ACK). An ACK is accomplished by the transmitting device first releasing the SDA line at the falling edge of the eighth clock cycle followed by the receiving device responding with a Logic 0 during the entire high period of the ninth clock cycle.

When the ZD24C02A/ZD24C04A/ZD24C08A/ZD24C16A is transmitting data to the Master, the Master can indicate that it is done receiving data and wants to end the operation by sending a Logic 1 response to the ZD24C02A/ZD24C04A/ZD24C08A/ZD24C16A instead of an ACK response during the ninth clock cycle. This is known as a no-acknowledge (NACK) and is accomplished by the Master sending a Logic 1 during the ninth clock cycle, at which point the ZD24C02A/ZD24C04A/ZD24C08A/ZD24C16A will release the SDA line so the Master can then generate a Stop condition.

The transmitting device, which can be the bus Master or the Serial EEPROM, must release the SDA line at the falling edge of the eighth clock cycle to allow the receiving device to drive the SDA line to a Logic 0 to ACK the previous 8-bit word. The receiving device must release the SDA line at the end of the ninth clock cycle to allow the transmitter to continue sending new data. A timing diagram has been provided in Figure 3-1 to better illustrate these requirements.

Figure 3-1.Start Condition, Data Transitions, Stop Condition and Acknowledge



3.4 Standby Mode

The ZD24C02A/ZD24C04A/ZD24C08A/ZD24C16A features a low-power standby mode which is enabled when any one of the following occurs:

- A valid power-up sequence is performed (see Section 8.5, “Pin Capacitance”).
- A Stop condition is received by the device unless it initiates an internal write cycle (see Section 5., “Write Operations”).
- At the completion of an internal write cycle (see Section 5.).
- An unsuccessful match of the device type identifier or hardware address in the Device Address byte occurs (see Section 4.1, “Device Addressing”).
- The bus Master does not ACK the receipt of data read out from the device; instead it sends a NACK response. (see Section 6., “Read Operations”).

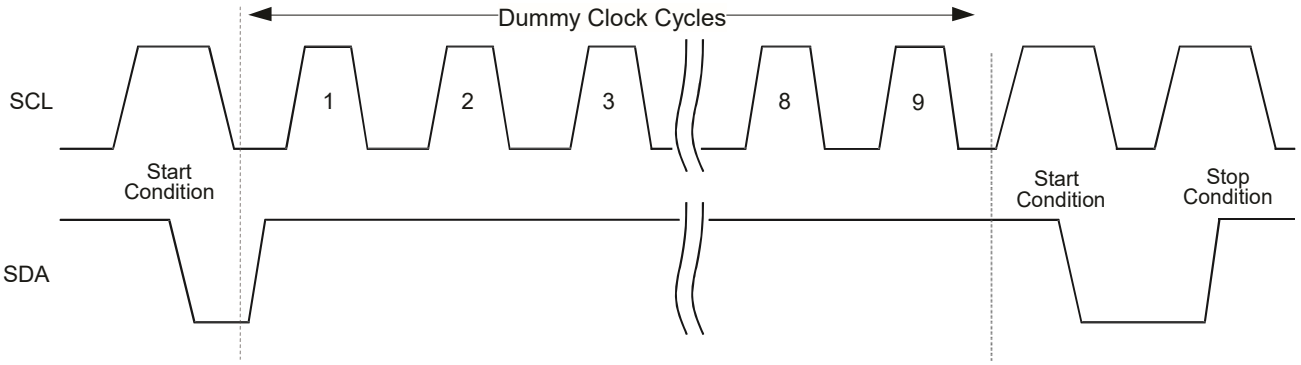
3.5 Software Reset

After an interruption in protocol, power loss, or system reset, any 2-wire part can be protocol reset by following these steps:

1. Create a Start condition (if possible).
2. Clock nine cycles.
3. Create another Start condition followed by a Stop condition as seen in Figure 3-2.

The device should be ready for the next communication after above steps have been completed. In the event that the device is still non-responsive or remains active on the SDA bus, a power cycle must be used to reset the device.

Figure 3-2. Software Reset



4. Memory Organization

ZD24C02A, 2K SERIAL EEPROM: Internally organized with 16 pages of 16 bytes each, the 2K requires an 8- bit data word address for random word addressing.

ZD24C04A, 4K SERIAL EEPROM: Internally organized with 32 pages of 16 bytes each, the 4K requires a 9- bit data word address for random word addressing.

ZD24C08A, 8K SERIAL EEPROM: Internally organized with 64 pages of 16 bytes each, the 8K requires a 10- bit data word address for random word addressing.

ZD24C16A, 16K SERIAL EEPROM: Internally organized with 128 pages of 16 bytes each, the 16K requires an 11-bit data word address for random word addressing.

4.1 Device Addressing

The 2K/4K/8K/16K EEPROM devices all require an 8-bit device address word following a start condition to enable the chip for a read or write operation (see Figure 4-1)

The device address word consists of a mandatory "1", "0" sequence for the first four most significant bits as shown. This is common to all the Serial EEPROM devices.

The next 3 bits are fixed to zero for the 2K EEPROM.

For the 4K EEPROM, the next two bits are fixed to zero and the third bit being a memory page address bit.

For the 8K EEPROM, the next one bit is fixed to zero and the next 2 bits being for memory page addressing.

The 16K does not use any device address bits but instead the 3 bits are used for memory page addressing. These page addressing bits on the 4K, 8K and 16K devices should be considered the most significant bits of the data word address which follows.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a "0". If a compare is not made, the chip will return to a standby state.

Figure 4-1. Device Address

	MSB							LSB
2K	1	0	1	0	0	0	0	R/W
4K	1	0	1	0	0	0	P0	R/W
8K	1	0	1	0	0	P1	P0	R/W
16K	1	0	1	0	P2	P1	P0	R/W

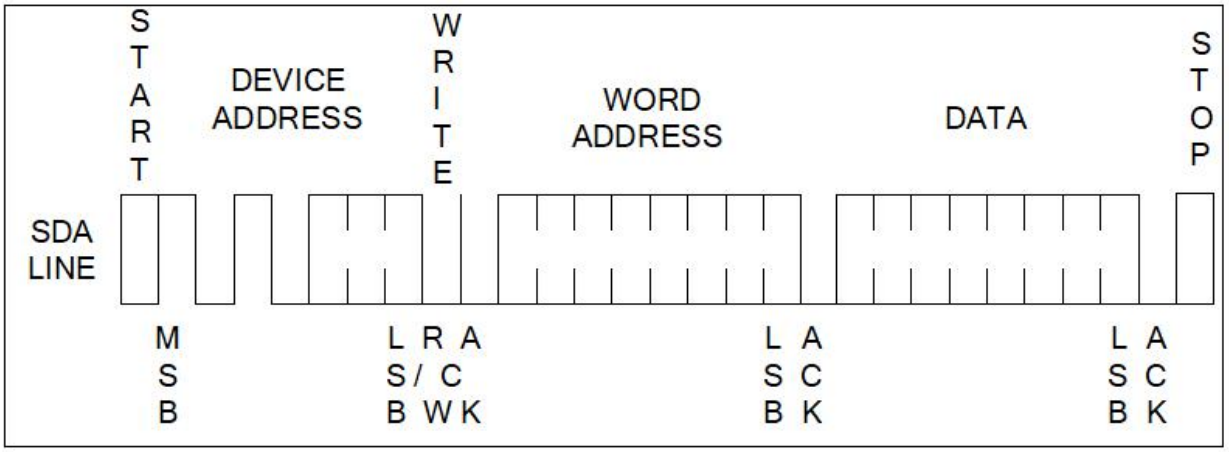
5. Write Operations

All write operations for the ZD24C02A/ZD24C04A/ZD24C08A/ZD24C16A begin with the Master sending a Start condition, followed by a Device Address byte with the R/W bit set to '0', and then by the Word Address byte. The data value(s) to be written to the device immediately follow the Word Address byte.

5.1 Byte Write

A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a "0" and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a "0" and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally timed write cycle, tWR, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see **Figure 5-1**)

Figure 5-1

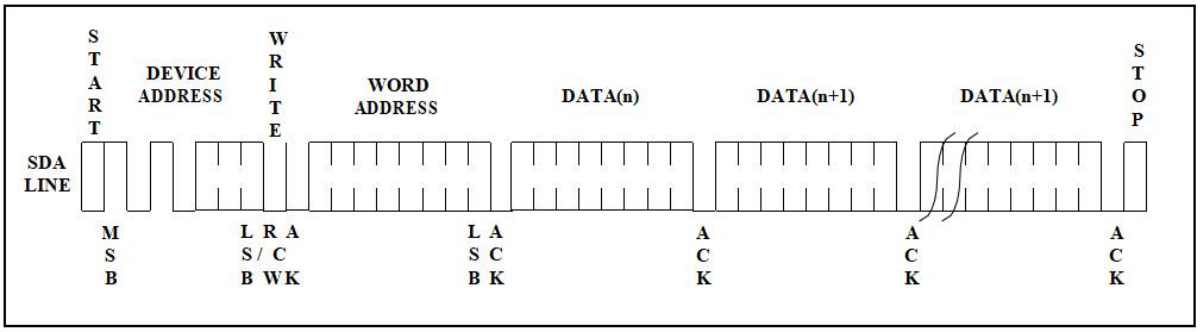


5.2 Page Write

A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to fifteen more data words. The EEPROM will respond with a "0" after each data word received. The microcontroller must terminate the page write sequence with a stop condition (see **Figure 5-2**).

The data word address lower four bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than sixteen data words are transmitted to the EEPROM, the data word address will "roll over" and previous data will be overwritten.

Figure 5-2

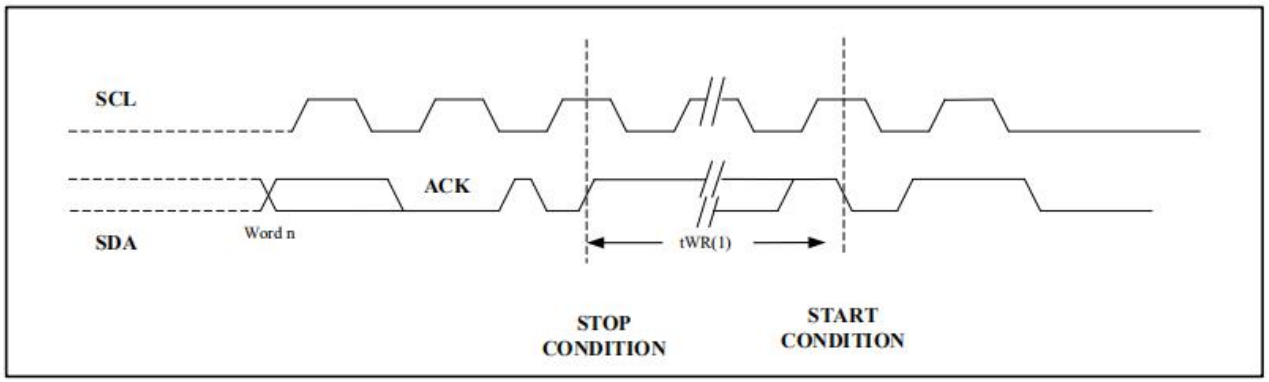


5.3 Acknowledge Polling

Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a "0", allowing the read or write sequence to continue.

5.4 Write Cycle Timing

Figure 5-4. SCL: Serial Clock, SDA: Serial Data I/O



Notes:
The write cycle time tWR is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

5.5 Write Protection

The ZD24C02A/ZD24C04A/ZD24C08A/ZD24C16A has a Write Protect pin that provides hardware data protection. The Write Protect pin allows normal read/write operations when connected to ground (GND). When the Write Protection pin is connected to Vcc, the write protection feature is enabled and operates as shown in the following **Table 5-5**

Table 5-5 Write Protect Behavior

WP Pin Voltage	Part of the Array Protected
Vcc	Full Array
GND	None — Write Protection Not Enabled

6. Read Operations

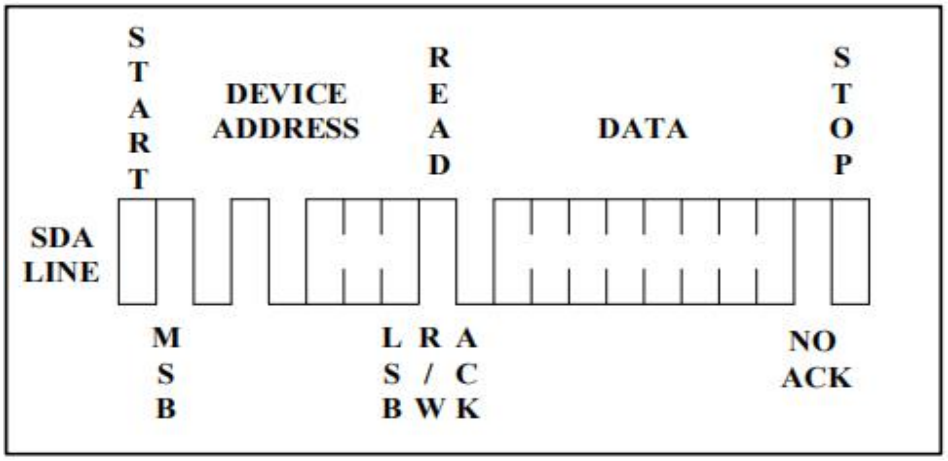
Read operations are initiated the same way as Write operations with the exception that the Read/Write Select bit in the Device Address word must be a Logic 1. There are three Read operations:

- Current Address Read
- Random Address Read
- Sequential Read

6.1 Current Address Read

The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to the first byte of the same page. Once the device address with the read/write select bit set to "1" is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input "0" but does generate a following stop condition (see Figure 6-1).

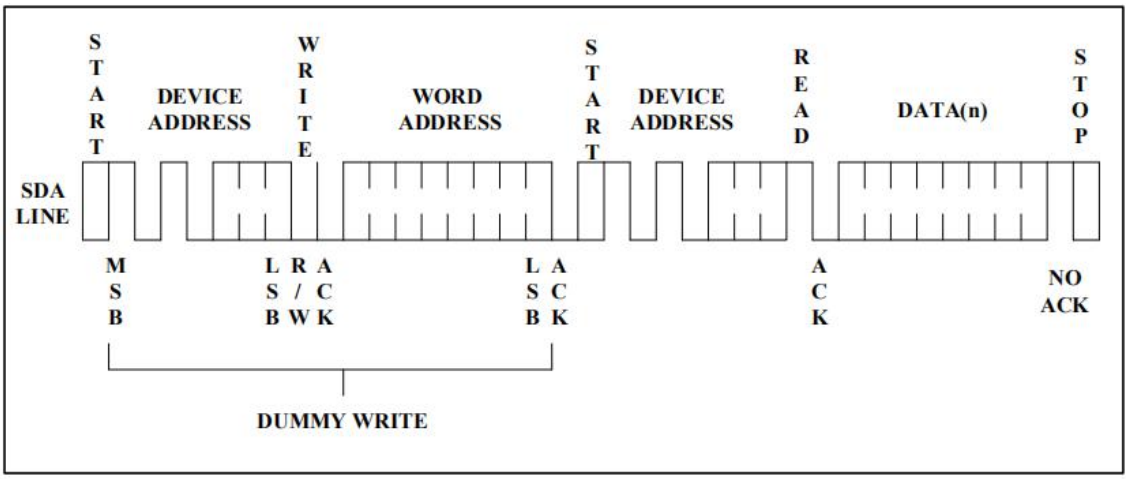
Figure 6-1



6.2 Random Read

A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a "0" but does generate a following stop condition (see **Figure 6-2**)

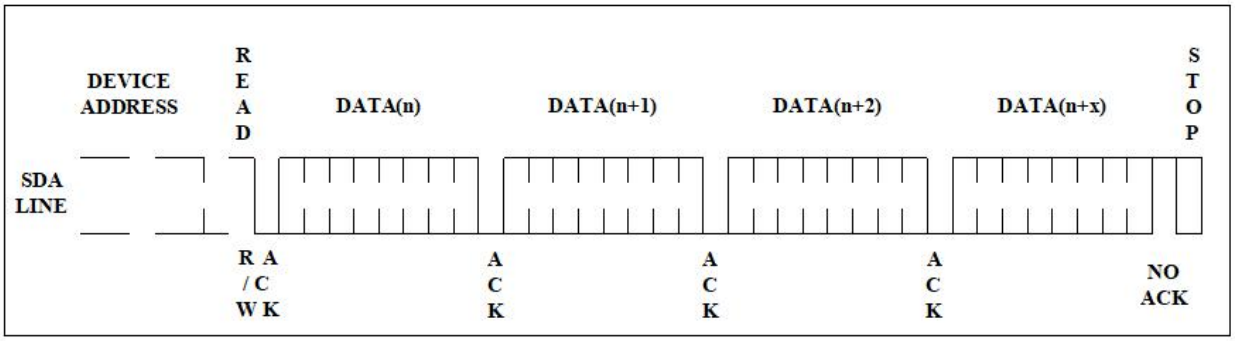
Figure 6-2



6.3 Sequential Read

Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a "0" but does generate a following stop condition (see **Figure 6-3**).

Figure 6-3



7. Device Default Condition from Zetta Device

The ZD24C02A/ZD24C04A/ZD24C08A/ZD24C16A is delivered with the EEPROM array set to Logic 1, resulting in FFh data in all locations.

8. Electrical Specifications

8.1 Absolute Maximum Ratings

- DC Supply Voltage.....-0.3V to +6.5V
- Input / Output Voltage.....GND-0.3V to VCC+0.3V
- Operating Ambient Temperature.....-40℃ to +85℃
- Storage Temperature.....-65℃ to +150℃
- Electrostatic pulse (Human Body model) 8000V

Comments:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

8.2 DC and AC Operating Range

Table 8-1.DC and AC Operating Range

Operating Temperature (Case)	Industrial Temperature Range	-40°C to +85°C
V_{CC} Power Supply	Low Voltage Grade	1.7V to 5.5V

8.3 DC Characteristics

Applicable over recommended operating range from: TA = -40℃ to +85℃, VCC = +1.7V to +5.5V (unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Supply Voltage	V_{CC1}	1.7	-	5.5	V	-
Supply Voltage	V_{CC2}	2.5	-	5.5	V	-
Supply Current VCC=5.0V	I_{CC1}	-	0.14	0.3	mA	READ at 400KHZ
Supply Current VCC=5.0V	I_{CC2}	-	0.28	0.5	mA	WRITE at 400KHZ
Supply Current VCC=5.0V	I_{SB1}	-	0.03	0.5	μA	V_{IN}=V_{CC} or V_{SS}
Input Leakage Current	I_{L1}	-	0.10	1.0	μA	V_{IN}=V_{CC} or V_{SS}
Output Leakage Current	I_{LO}	-	0.05	1.0	μA	V_{OUT}=V_{CC} or V_{SS}
Input Low Level	V_{IL1}	-0.3	-	V_{CC}×0.3	V	V_{CC}=1.7V to 5.5V
Input High Level	V_{IH1}	V_{CC}×0.7	-	V_{CC}+0.3	V	V_{CC}=1.7V to 5.5V
Output Low Level VCC=1.7V	V_{OL1}	-	-	0.2	V	I_{OL}=0.15mA
Output Low Level VCC=5.0V	V_{OL2}	-	-	0.4	V	I_{OL}=3.0mA

8.4 AC Characteristics

Applicable over recommended operating range from TA = -40℃ to +85℃, VCC = +1.7V to +5.5V, CL = 1 TTL Gate and 100 pF (unless otherwise noted)

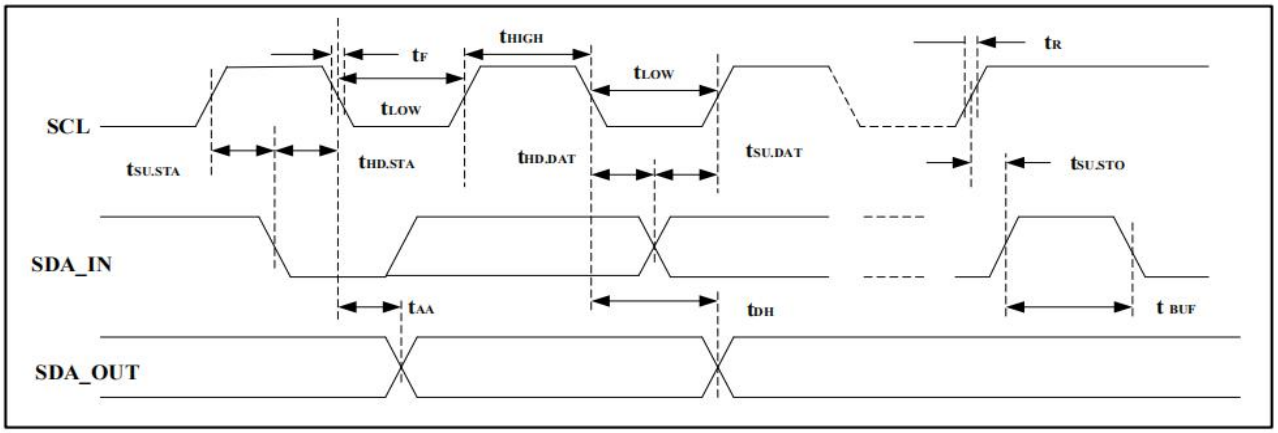
Parameter	Symbol	1.7V≤VCC < 2.5V			2.5V≤VCC < 5.5V			Units
		Min	Typ	Max	Min	Typ	Max	
Clock Frequency,SCL	fSCL	-	-	400	-	-	1000	KHZ
Clock Pulse Width Low	tLOW	0.6	-	-	0.6	-	-	μs
Clock Pulse Width High	tHIGH	0.4	-	-	0.4	-	-	μs
Noise Suppression Time	tI	-	-	50	-	-	50	ns
Clock Low to Data Out Valid	tAA	0.1	-	0.55	0.1	-	0.55	μs
Time the bus must be free before a new transmission can start	tBUF	0.5	-	-	0.5	-	-	μs
Start Hold Time	tHD:STA	0.25	-	-	0.25	-	-	μs
Start Setup Time	tSU:DAT	0.25	-	-	0.25	-	-	μs
Data In Hold Time	tHD:DAT	0	-	-	0	-	-	μs
Data in Setup Time	tSU:DAT	100	-	-	100	-	-	ns
Input Rise Time(1)	tR	-	-	0.3	-	-	0.3	μs
Input Fall Time(1)	tF	-	-	0.3	-	-	0.3	μs
Stop Setup Time	tSu:STO	0.25	-	-	0.25	-	-	μs
Data Out Hold Time	tDH	50	-	-	50	-	-	ns
Write Cycle Time	twR	-	1.9	3	-	1.9	3	ms
5.0V,25℃,Byte Mode(1)	Endurance	1M	-	-	-	-	-	Write Cycle

Notes:

1. This parameter is characterized and is not 100% tested.
2. AC measurement conditions:
   RL (connects to VCC): 1.3 k
   Input pulse voltages: 0.3 VCC to 0.7 VCC
   Input rise and fall time: 50 ns
   Input and output timing reference voltages: 0.5 VCC
   The value of RL should be concerned according to the actual loading on the user's system.

Bus Timing(Figure 8-4)

Figure 8-4. SCL: Serial Clock, SDA: Serial Data I/O

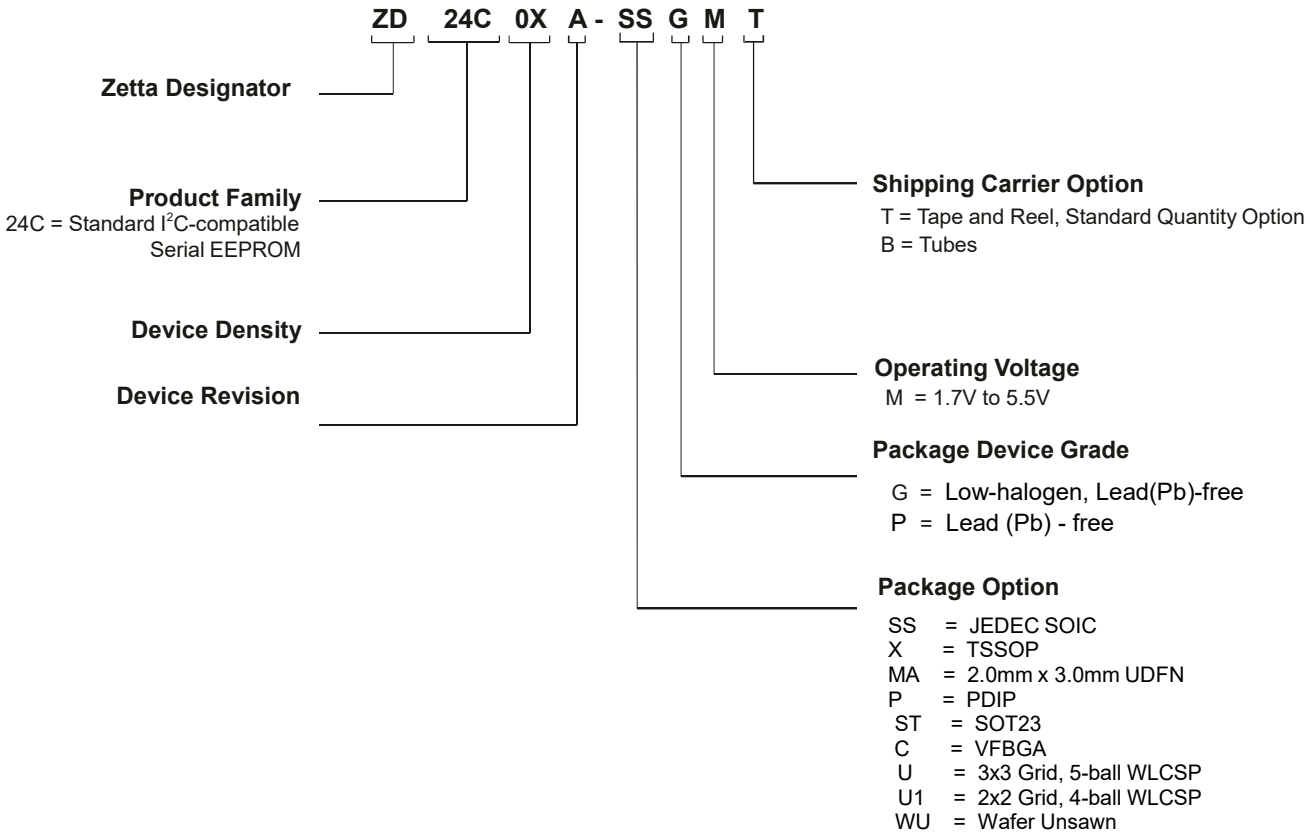


8.5 Pin Capacitance

Applicable over recommended operating range from TA = 25℃, f = 1.0 MHz, VCC = +1.7V

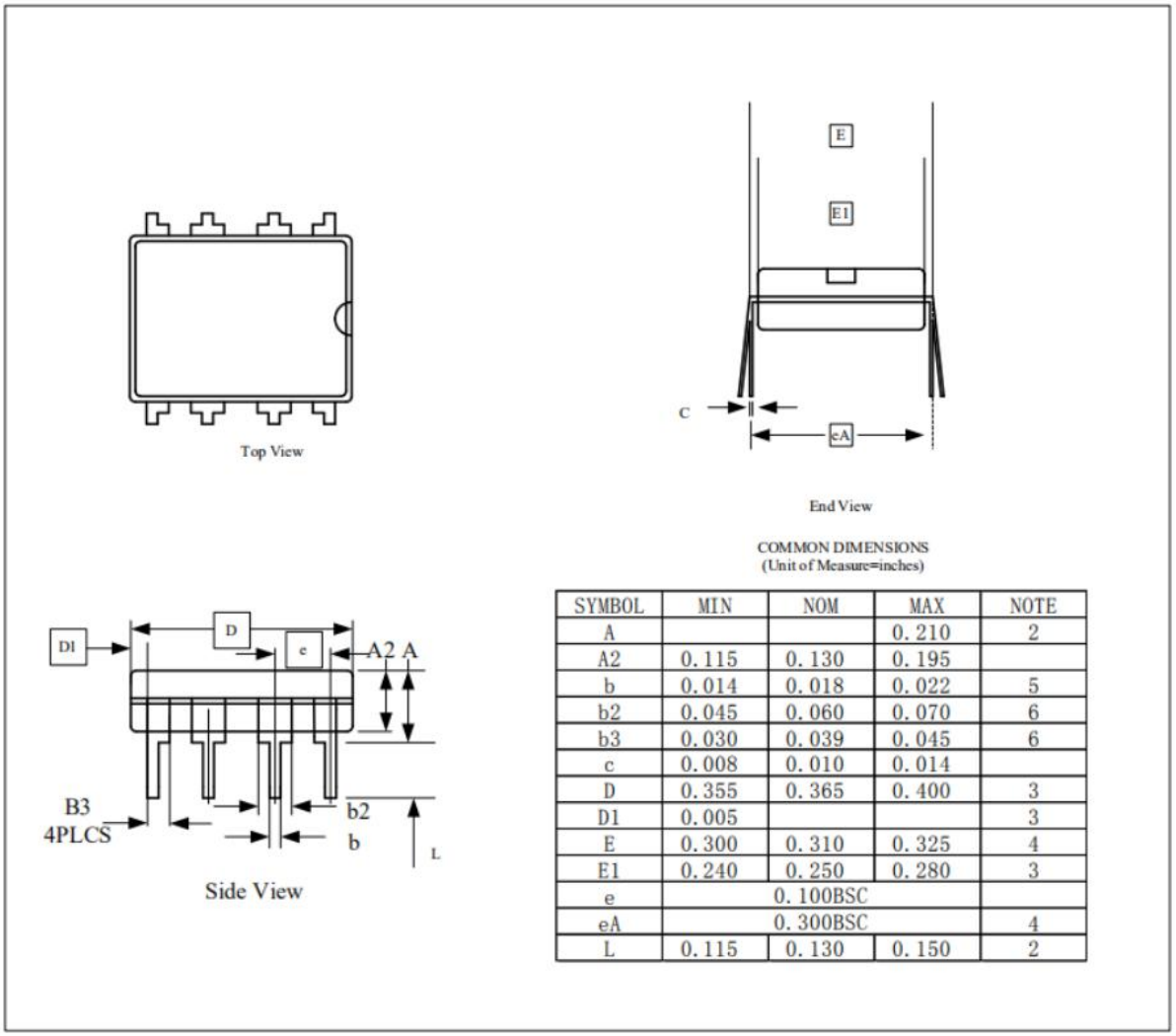
Parameter	Symbol	Min	Typ	Max	Unit	Condition
Input/Output Capacitance(SDA)	$C_{I/O}$	-	-	8	pF	V_{IO}=0V
Input Capacitance(A0,A1,A2,SCL)	C_{IN}	-	-	6	pF	V_{IN}=0V

9. Ordering Information



10 Packaging Information

10.1 PDIP Outline Dimensions

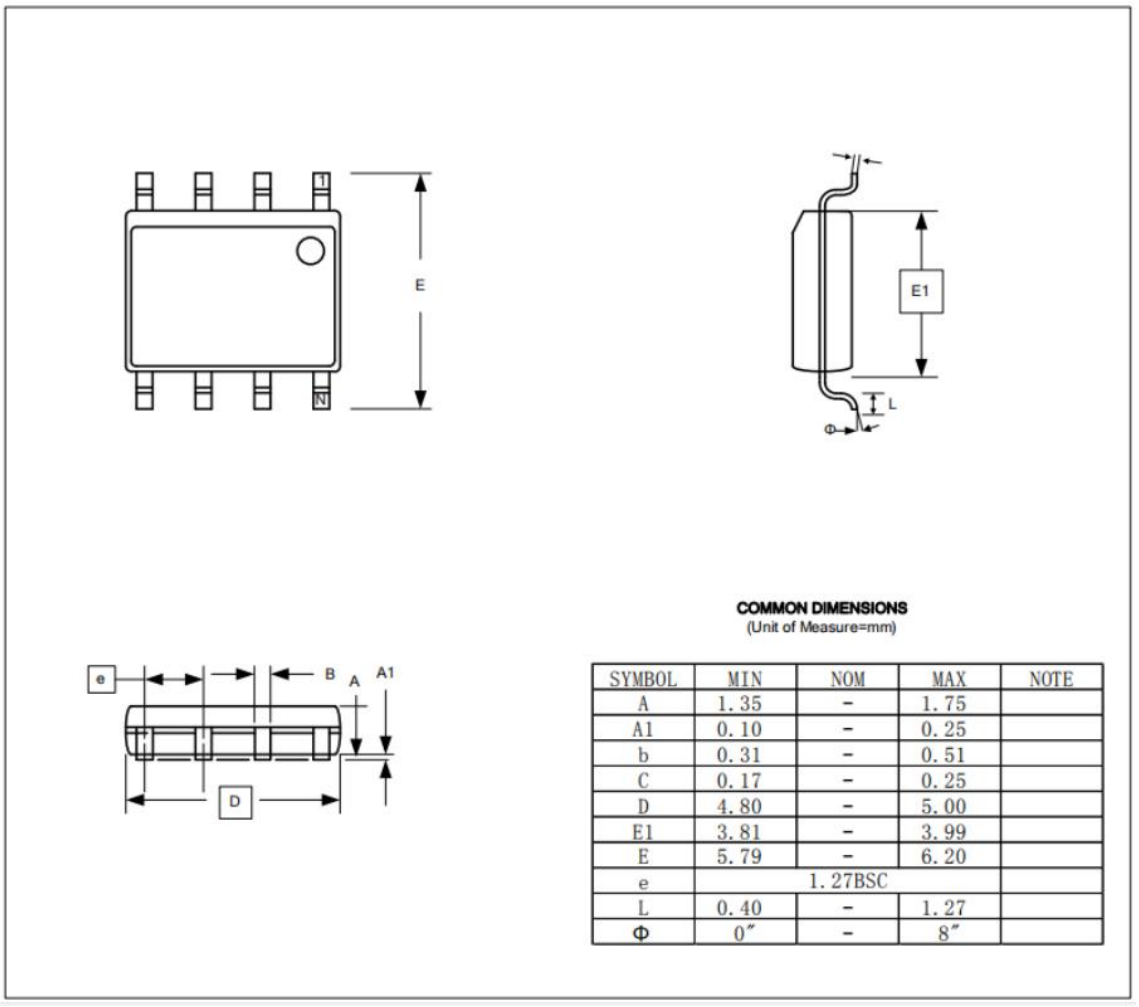


COMMON DIMENSIONS
(Unit of Measure=inches)

SYMBOL	MIN	NOM	MAX	NOTE
A			0.210	2
A2	0.115	0.130	0.195	
b	0.014	0.018	0.022	5
b2	0.045	0.060	0.070	6
b3	0.030	0.039	0.045	6
c	0.008	0.010	0.014	
D	0.355	0.365	0.400	3
D1	0.005			3
E	0.300	0.310	0.325	4
E1	0.240	0.250	0.280	3
e		0.100BSC		
eA		0.300BSC		4
L	0.115	0.130	0.150	2

Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-001, Variation BA for additional information.
2. Dimensions A and L are measured with the package seated in JEDEC seating plane Gauge GS-3.
3. D, D1 and E1 dimensions do not include mold Flash or protrusions. Mold Flash or protrusions shall not exceed 0.010 inch.
4. E and eA measured with the leads constrained to be perpendicular to datum.
5. Pointed or rounded lead tips are preferred to ease insertion.
6. b2 and b3 maximum dimensions do not include Dambar protrusions. Dambar protrusions shall not exceed 0.010 (0.25 mm).

10.2 SOP



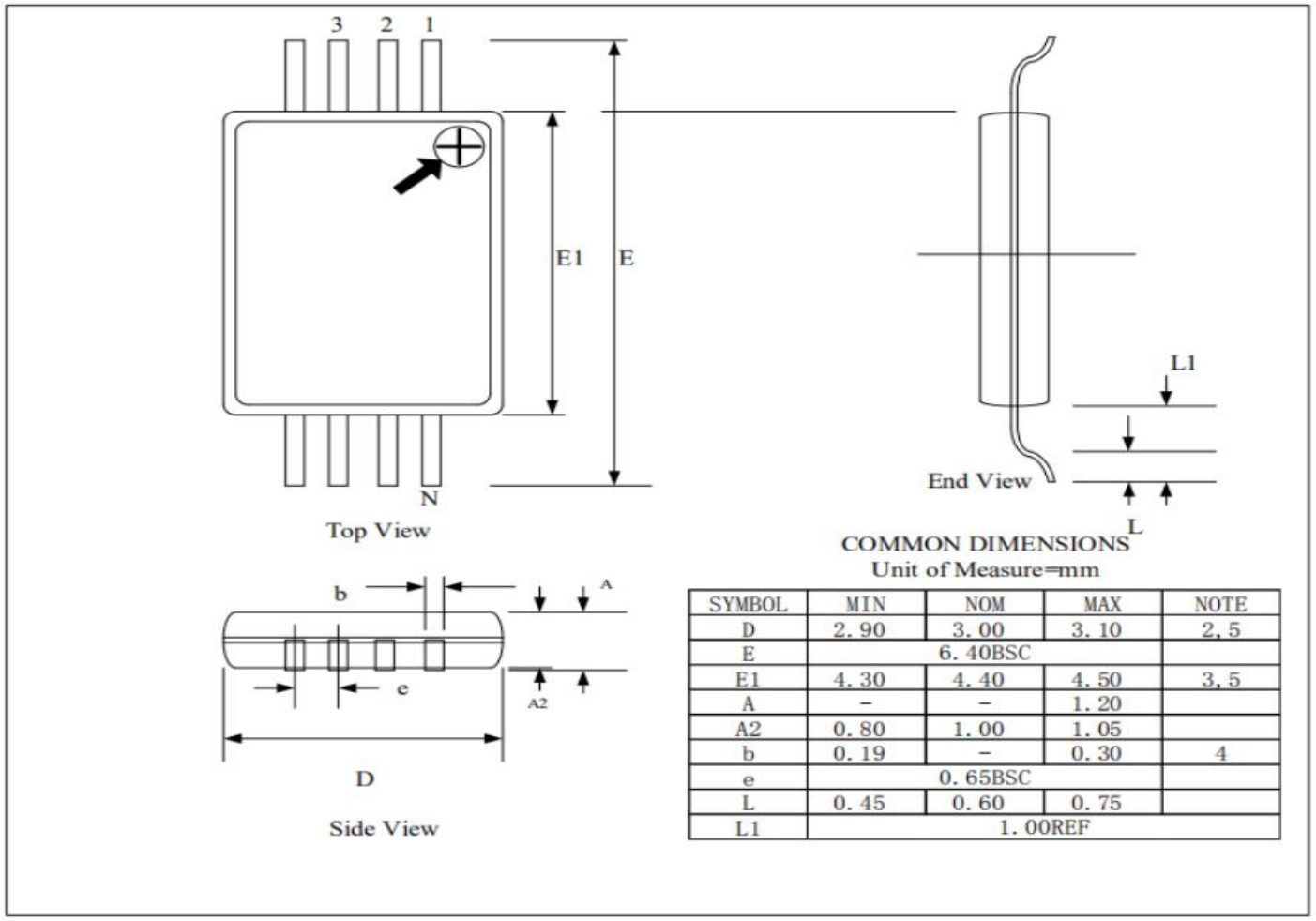
COMMON DIMENSIONS
(Unit of Measure=mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	-	1.75	
A1	0.10	-	0.25	
b	0.31	-	0.51	
C	0.17	-	0.25	
D	4.80	-	5.00	
E1	3.81	-	3.99	
E	5.79	-	6.20	
e	1.27BSC			
L	0.40	-	1.27	
Φ	0°	-	8°	

Notes:

These drawings are for general information only. Refer to JEDEC Drawing MS-012, Variation AA for proper dimensions, tolerances, datums, etc.

10.3 TSSOP



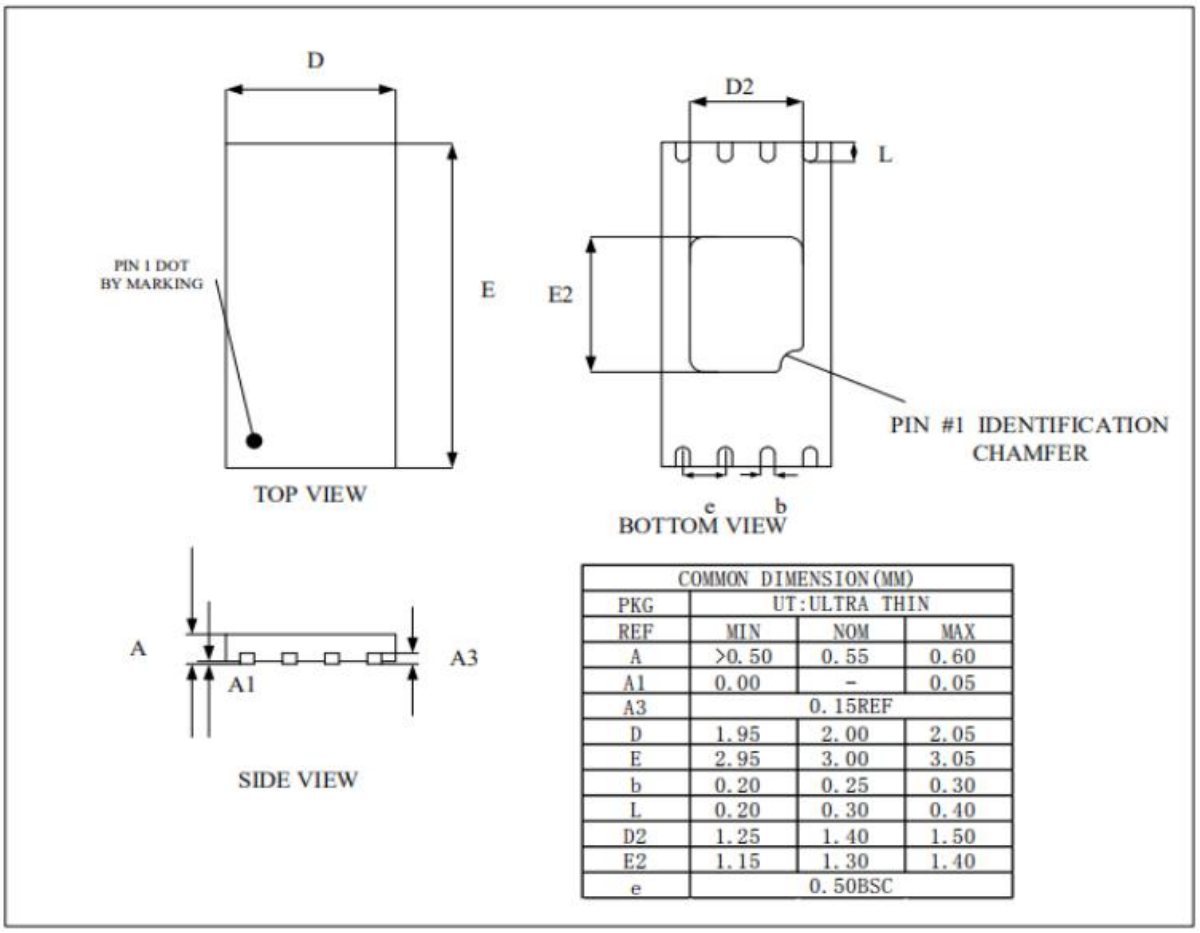
COMMON DIMENSIONS
Unit of Measure=mm

SYMBOL	MIN	NOM	MAX	NOTE
D	2. 90	3. 00	3. 10	2, 5
E		6. 40BSC		
E1	4. 30	4. 40	4. 50	3, 5
A	–	–	1. 20	
A2	0. 80	1. 00	1. 05	
b	0. 19	–	0. 30	4
e		0. 65BSC		
L	0. 45	0. 60	0. 75	
L1		1. 00REF		

Notes:

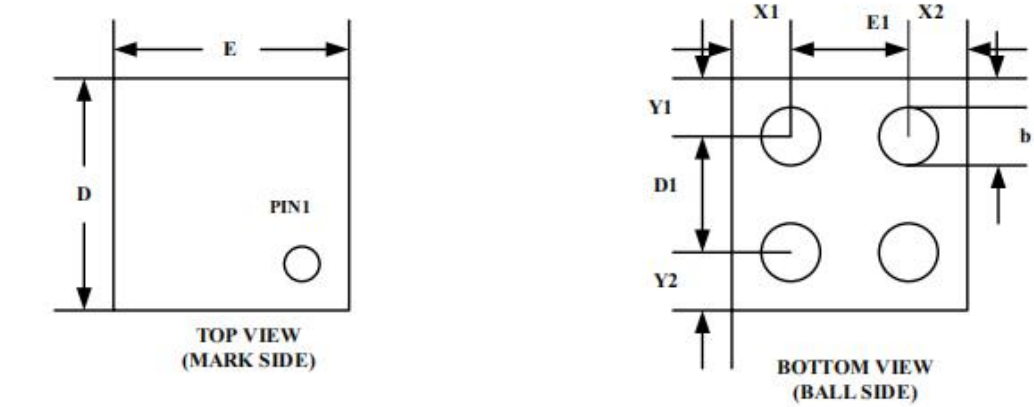
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006 in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010 in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximummaterial condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07 mm.
5. Dimension D and E1 to be determined at Datum Plane H.

10.4 UDFN



COMMON DIMENSION(MM)			
PKG	UT:ULTRA THIN		
REF	MIN	NOM	MAX
A	>0.50	0.55	0.60
A1	0.00	-	0.05
A3	0.15REF		
D	1.95	2.00	2.05
E	2.95	3.00	3.05
b	0.20	0.25	0.30
L	0.20	0.30	0.40
D2	1.25	1.40	1.50
E2	1.15	1.30	1.40
e	0.50BSC		

10.5 WLCSP



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.270	0.290	0.310
A1	0.045	0.055	0.065
A2	0.215	0.235	0.255
D	0.738	0.758	0.778
D1		0.400BSC	
E	0.668	0.688	0.708
E1		0.400BSC	
b	0.160	0.180	0.200
x1		0.144 REF	
x2		0.144 REF	
y1		0.179 REF	
y2		0.179 REF	

NOTES: All wafer orientation notch down.

11. Revision History

Rev.	Date	Description
1.0	2019-10-10	Initial Release
1.1	2020-01-02	Modify Package Information