I2C-Compatible (2-wire) Serial EEPROM

256K-bit

DATASHEET

Features

- Compatible with all I2C bidirectional data transfer protocol
- Memory array:
  - 256 Kbits (32 Kbytes) of EEPROM
  - Page size: 64 bytes
  - Additional Write lockable page
- Single supply voltage and high speed:
  - 1 MHz
- Random and sequential Read modes
- Write:
  - Byte Write within 3 ms
  - Page Write within 3 ms
  - Partial Page Writes Allowed
- Write Protect Pin for Hardware Data Protection
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- High-reliability
  - Endurance: 1 Million Write Cycles
  - Data Retention: 100 Years
- Enhanced ESD/Latch-up protection
  - HBM 6000V
- 8-lead PDIP/SOP/TSSOP/UDFN/TSOT23-5 packages

Description

- The ZD24C256A provides 262144 bits of serial electrically erasable and programmable read-only memory (EEPROM), organized as 32768 words of 8 bits each.
- The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential.
- The ZD24C256A offers an additional page, named the Identification Page (64 bytes). The Identification Page can be used to store sensitive application parameters which can be (later) permanently locked in Read-only mode

1. Pin Descriptions and Pinouts

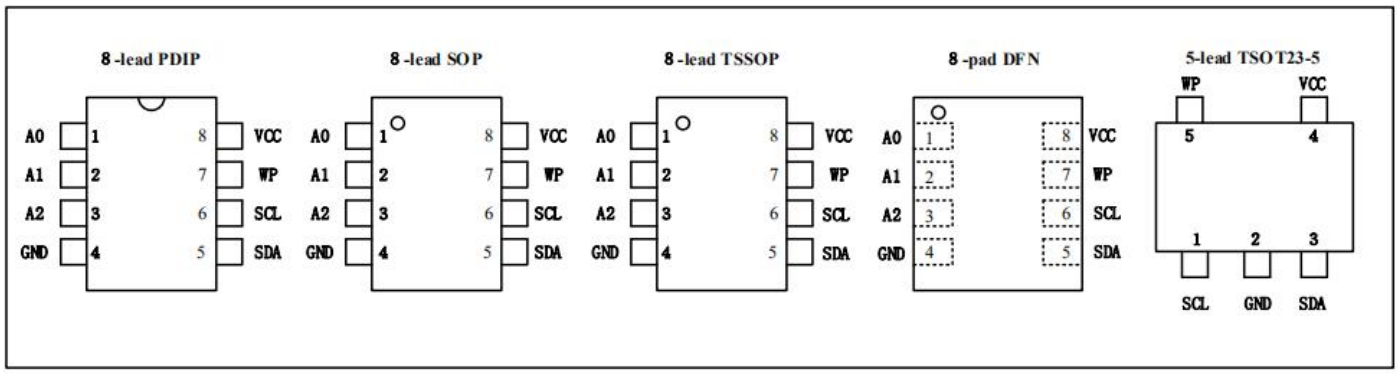


Table 1-1.Pin Descriptions

A0,A1,A2	Input	Slave Address Setting
Vss	Ground	Ground
SDA	I/O	Serial Data Input and Serial Data Output
SCL	Input	Serial Clock Input
WP	Input	Write Control, Low Enable Write
Vcc	Power	Power

Serial Clock (SCL): The SCL input is used to positive-edge clock data in and negative-edge clock data out of each device.

Serial Data (SDA) : The SDA pin is bidirectional for serial data transfer. This pin is open drain driven and may be wire-OR'ed with any number of other open-drain or open-collector devices.

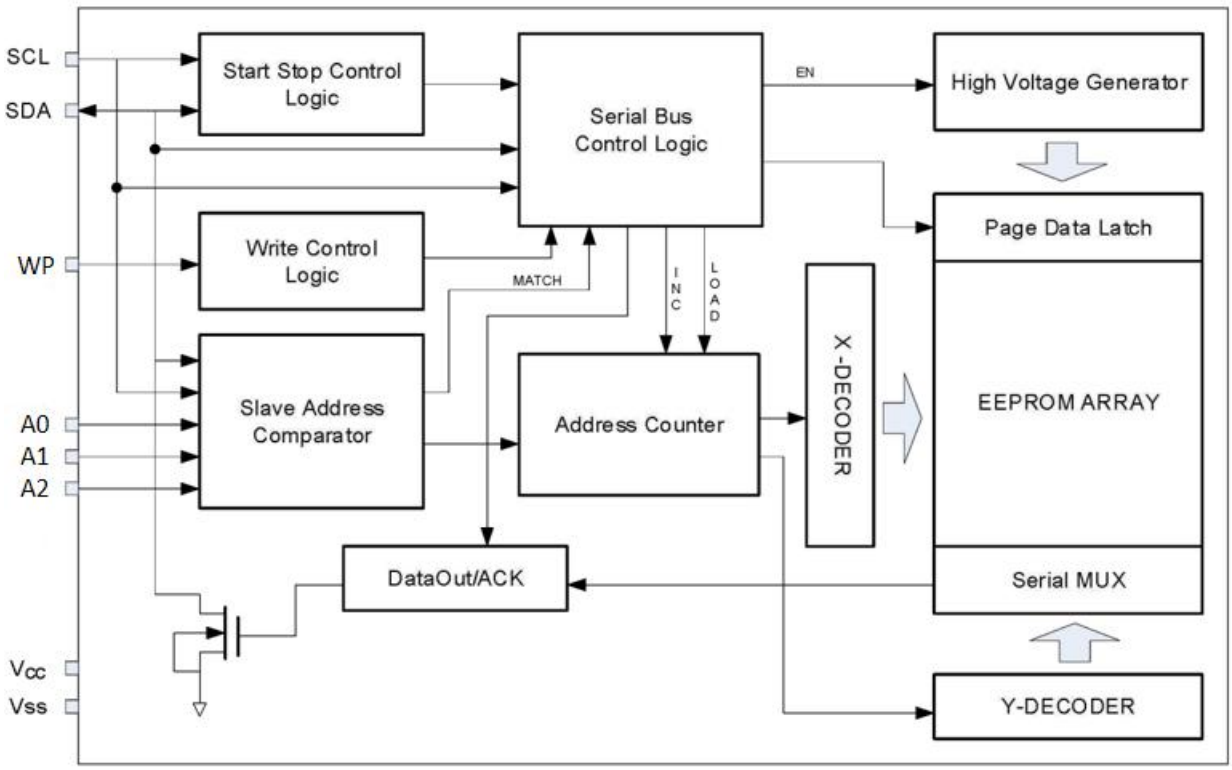
Write Control (WP): The Write Control input, when WP is connected directly to V_{CC}, all write operations to the memory are inhibited. When connected to Vss, allows normal write operations. If the pin is left floating, the WP pin will be internally pulled down to Vss. As shown in the following table1.

Device Addresses (A2, A1, A0): The A2, A1, and A0 pins are device address inputs. Typically, the A2, A1, and A0 pins are for hardware addressing and a total of 8 devices can be connected on a single bus system. If these pins are left floating, the A2, A1, and A0 pins will be internally pulled down to Vss.

WP Pin Status	ZD24C256A
At VCC	Full(256K)Array
At GND	Normal Read/Write Operations

Table1

2. Device Block Diagram and System Configuration



3.Functional Description

1. Memory Organization

ZD24C256A, 256K SERIAL EEPROM: Internally organized with 512 pages of 64 bytes each, the 256K requires a 15-bit data word address for random word addressing.

2. Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see **Figure 2**). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see **Figure 3**).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (see **Figure 3**).

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a "0" to acknowledge that it has received each word. This happens during the ninth clock cycle.(see **Figure 4**).

STANDBY MODE: The ZD24C256A features a low-power standby mode which is enabled:

1. After a fresh power up.
2. After receiving a STOP bit in read mode.
3. After completing a self-time internal programming operation.

MEMORY RESET: After an interruption in protocol, power loss or system reset, any two-wire part can be reset by following these steps:

1. Clock up to 9 cycles.
2.Look for SDA high in each cycle while SCL is high.
3.Create a start condition.

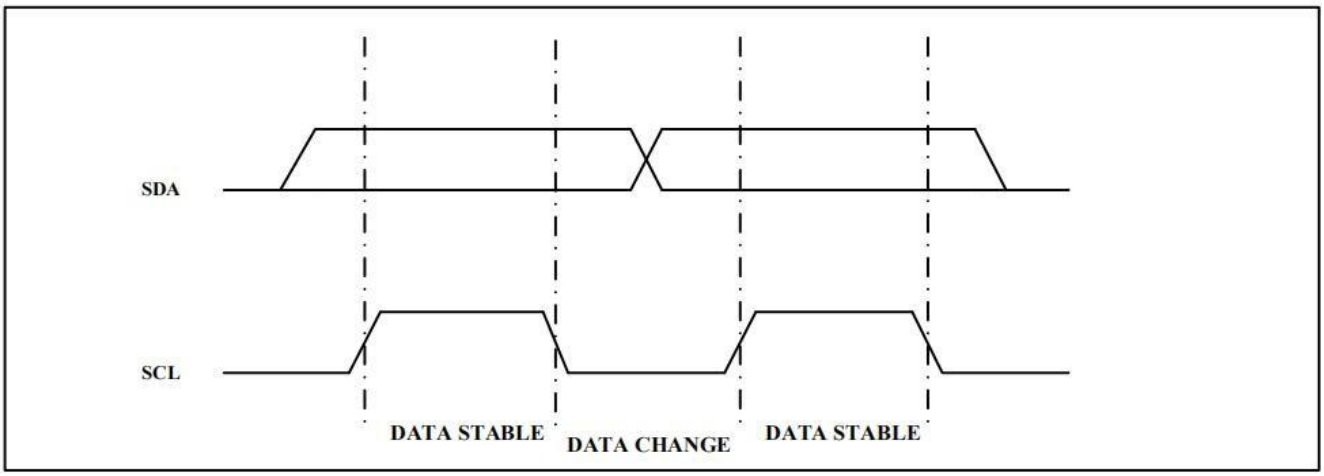


Figure 2. Data Validity

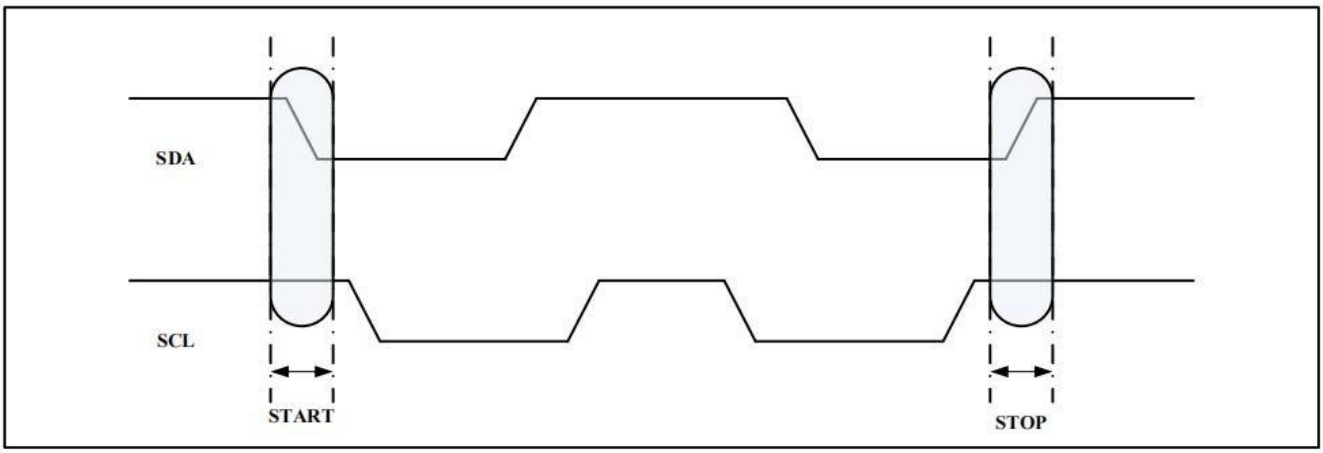


Figure 3. Start and Stop Definition

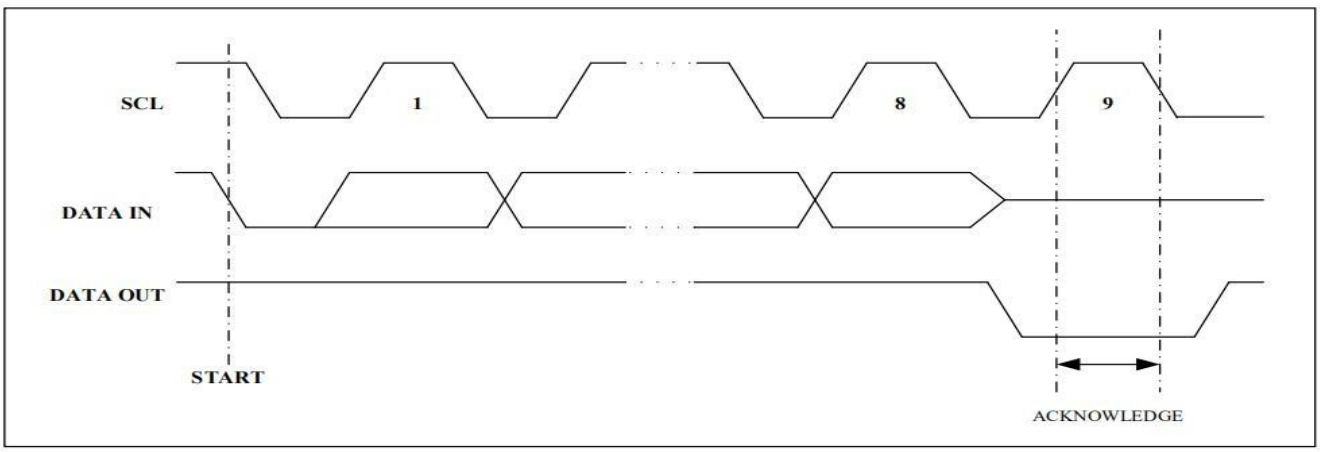


Figure 4. Output Acknowledge

4.Device Addressing

The 256K EEPROM devices all require an 8-bit device address word following a start condition to enable the chip for a read or write operation (see **Figure 5**)

The device address word consists of a mandatory "1", "0" sequence for the first four most significant bits as shown. This is common to all the Serial EEPROM devices.

The 256K EEPROM uses A2, A1 and A0 device address bits to allow as much as eight devices on the same bus. These 3 bits must be compared to their corresponding hardwired input pins. The A2, A1 and A0 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are allowed to float.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a "0". If a compare is not made, the chip will return to a standby state.

DATA SECURITY: The ZD24C256A has a hardware data protection scheme that allows the user to write protect the entire memory when the WP pin is at VCC.

MSB							LSB
1	0	1	0	A2	A1	A0	R/W

Figure 5: Device Address

5.Write Operations

BYTE WRITE:

A write operation requires two 8-bit data word address following the device address word and acknowledgment. Upon receipt of every 8-bit address, the EEPROM will again respond with a "0" and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a "0" and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally timed write cycle, tWR, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see **Figure 6**).

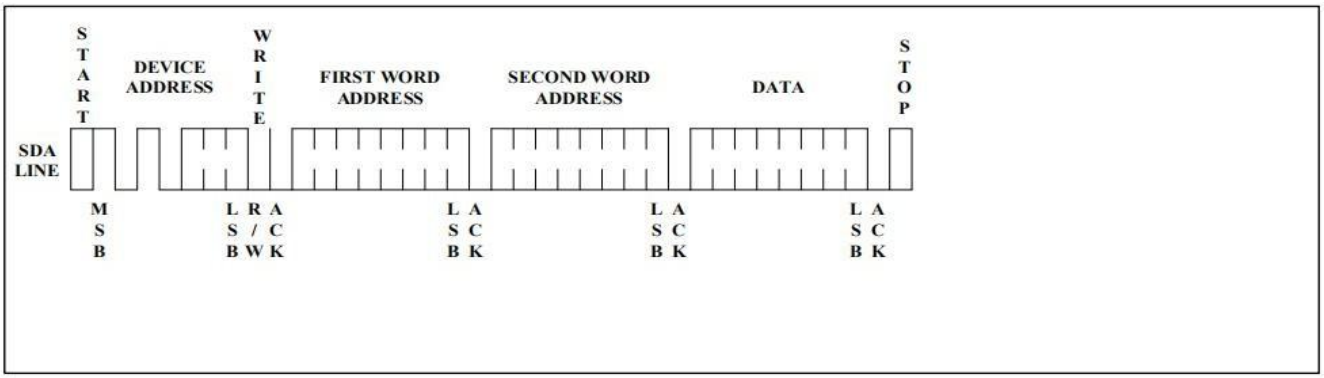


Figure 6. Byte Write

PAGE WRITE:

The 256K EEPROM is capable of a 64-byte page writes. A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 63 more data words. The EEPROM will respond with a “0” after each data word received. The microcontroller must terminate the page write sequence with a stop condition (see **Figure 7**).

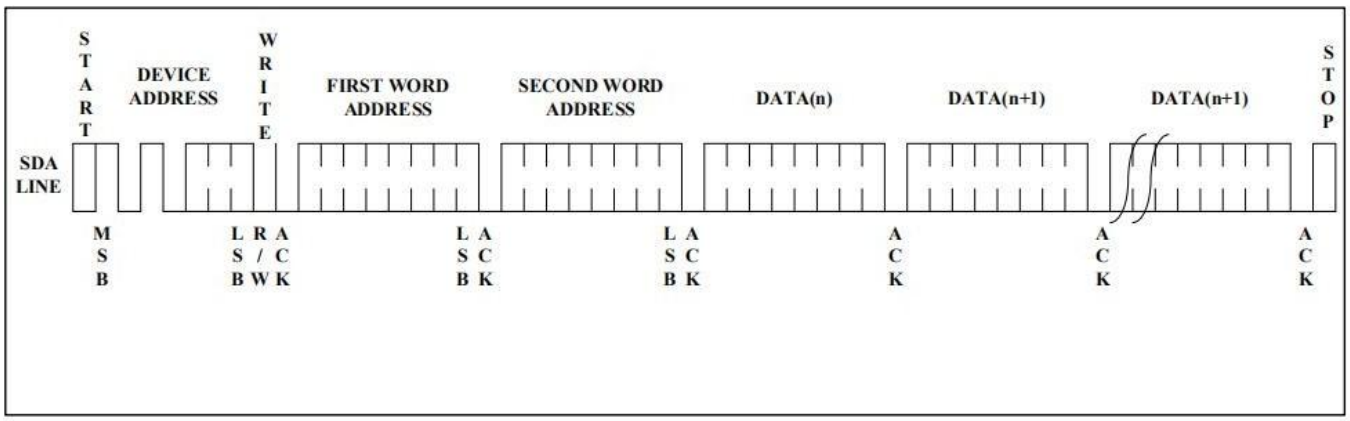


Figure 7. Page Write

The data word address lower six bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 64 data words are transmitted to the EEPROM, the data word address will "roll over" and previous data will be overwritten.

WRITE IDENTIFICATION PAGE:

The Identification Page (64 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode. It is written by issuing the Write Identification Page instruction. This instruction uses the same protocol and format as Page Write (into memory array), except for the following differences:

Device type identifier = 1011b

MSB address bits B15/B6 are don't care except for address bit B10 which must be "0".

LSB address bits B5/B0 define the byte address inside the Identification page.

If the Identification page is locked, the data bytes transferred during the Write Identification Page instruction are not acknowledged (NoAck).

ACKNOWLEDGE POLLING:

Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a "0", allowing the read or write sequence to continue.

6.Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to "1". There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ:

The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to the first byte of the same page.

Once the device address with the read/write select bit set to "1" is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input "0" but does generate a following stop condition (see **Figure 8**).

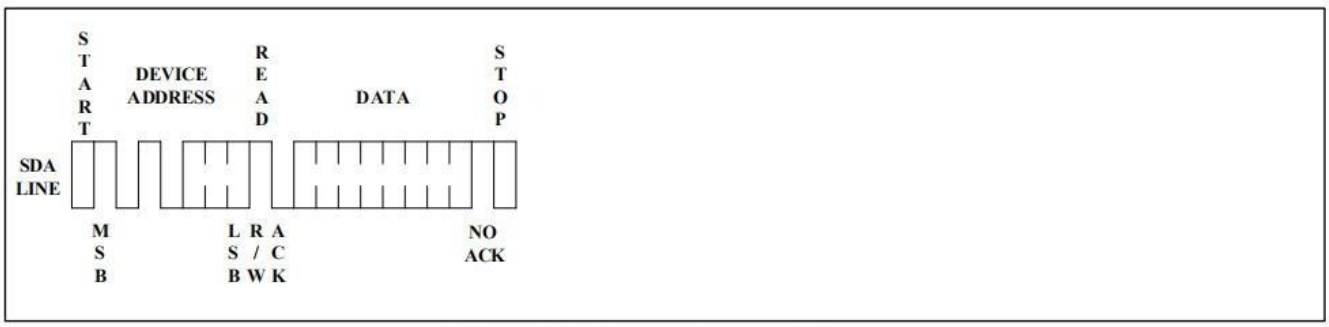


Figure 8. Current Address Read

RANDOM READ:

A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a "0" but does generate a following stop condition (see **Figure 9**)

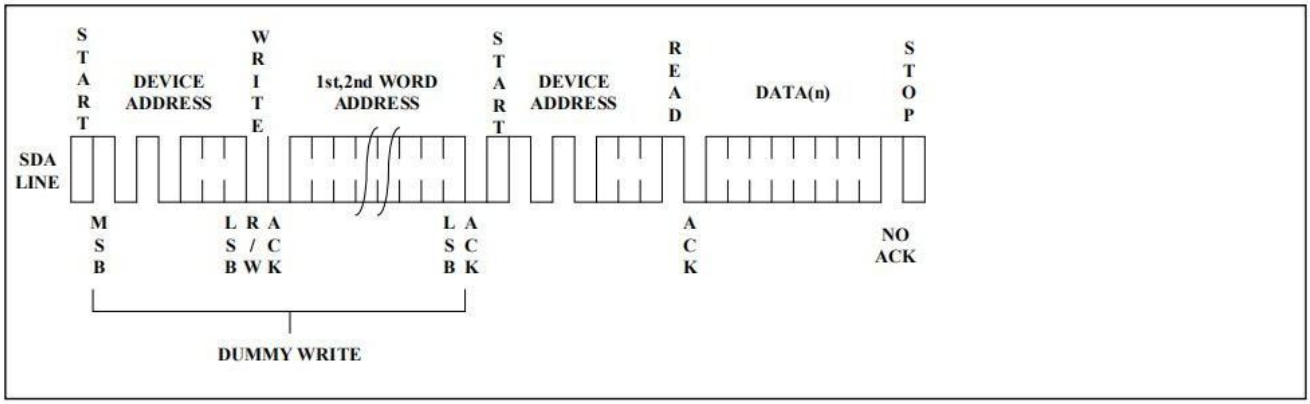


Figure 9. Random Read

SEQUENTIAL READ:

Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a "0" but does generate a following stop condition (see **Figure 10**).

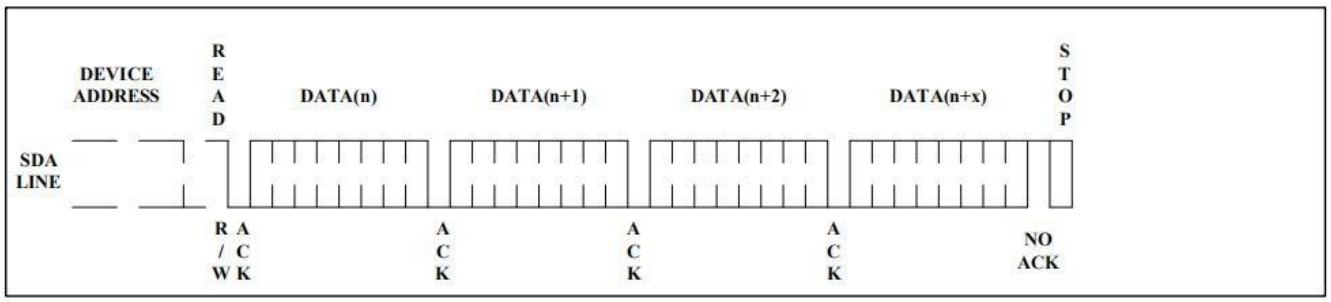


Figure 10. Sequential Read

READ IDENTIFICATION PAGE: The Identification Page (64 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode.

The Identification Page can be read by issuing a Read Identification Page instruction. This instruction uses the same protocol and format as the Random Address Read (from memory array) with device type identifier defined as 1011b. The MSB address bits B15/B6 are don't care, the LSB address bits B5/B0 define the byte address inside the Identification Page. The number of bytes to read in the ID page must not exceed the page boundary (e.g.: when reading the Identification Page from location 10d, the number of bytes should be less than or equal to 54, as the ID page boundary is 64 bytes)

LOCK IDENTIFICATION PAGE: The Lock Identification Page instruction (Lock ID) permanently locks the Identification page in Read-only mode. The Lock ID instruction is similar to Byte Write (into memory array) with the following specific conditions:

Device type identifier = 1011b

Address bit B10 must be '1'; all other address bits are don't care

The data byte must be equal to the binary value xxxx xx1x, where x is don't care

7.Electrical Characteristics

Absolute Maximum Stress Ratings:

- DC Supply Voltage..... -0.5V to +6.25V
- Input / Output Voltage.....-0.5V to +6.25V
- Operating Ambient Temperature..... -40℃ to +105℃
- Storage Temperature..... -65℃ to +150℃
- DC output current(SDA=0).....5mA

Comments:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

Applicable over recommended operating range from: TA = -40℃ to +105℃, VCC = +1.7V to +5.5V
(unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{CC}	Supply Voltage	1.7	-	5.5	V	
		1.8	-	5.5	V	
		2.5	-	5.5	V	
		-	-	3.0	uA	Vcc = 5.5V, T_A = 85°C
		-	-	6.0	uA	Vcc = 5.5V, T_A = 105°C
I_{CC1}	Supply Current	-	0.2	0.4	mA	Vcc=5.5V, Read at 400Khz
I_{CC2}	Supply Current	-	0.8	1.6	mA	Vcc=5.5V Write at 400Khz
I_{LI}	Input Leakage Current	-	0.10	1.0	μA	V_{IN} = V_{CC} or Vss
I_{LO}	Output Leakage Current	-	0.05	1.0	μA	V_{OUT} = V_{CC} or Vss
V_{IL}	Input Low Level	–0.6	-	$0.3V_{CC}$	V	
V_{IH}	Input High Level	$0.7V_{CC}$	-	V_{CC}+0.5	V	
V_{OL1}	Output Low Level V_{CC} = 1.7V (SDA)	-	-	0.2	V	I_{OL} = 1.5 mA
V_{OL2}	Output Low Level V_{CC} = 3.0V (SDA)	-	-	0.4	V	I_{OL} = 2. 1 mA

Table3

Pin Capacitance

Applicable over recommended operating range from TA = 25℃, f = 1.0 MHz, VCC = +1.7V

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Input/Output Capacitance(SDA)	$C_{I/O}$	-	-	8	pF	V_{IO}=0V
Input Capacitance(A0,A1,A2,SCL)	C_{IN}	-	-	6	pF	V_{IN}=0V

Table 4

8.AC Electrical Characteristics

Applicable over recommended operating range from TA = -40℃ to +105℃, VCC = +1.7V to +5.5V, CL = 1 TTL Gate and 100 pF (unless otherwise noted)

Symbol	Parameter	1.7≤V_{CC}<5.5			2.5≤V_{CC}≤5.5			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{SCL}	Clock Frequency, SCL	-	-	400	-	-	1000	kHz
t_{LOW}	Clock Pulse Width Low	1.3	-	-	0.4	-	-	μs
t_{HIGH}	Clock Pulse Width High	0.6	-	-	0.4	-	-	μs
t_{AA}	Clock Low to Data Out Valid	0.05	-	0.9	0.05	-	0.55	μs
t_I	Noise Suppression Time	-	-	0.1	-	-	0.05	μs
t_{BUF}	Time the bus must be free before a new transmission can start	1.3	-	-	0.5	-	-	μs
$t_{HD.STA}$	Start Hold Time	0.6	-	-	0.25	-	-	μs
$t_{SU.STA}$	Start Setup Time	0.6	-	-	0.25	-	-	μs
$t_{HD.DAT}$	Data In Hold Time	0	-	-	0	-	-	μs
$t_{SU.DAT}$	Data In Setup Time	0.1	-	-	0.1	-	-	μs
t_R	Inputs Rise Time[1]	-	-	0.3	-	-	0.3	μs
t_F	Inputs Fall Time[1]	-	-	0.3	-	-	0.1	μs
$t_{SU.STO}$	Stop Setup Time	0.6	-	-	0.25	-	-	μs
t_{DH}	Data Out Hold Time	0.05	-	-	0.05	-	-	μs
$t_{SU.WP}$	WP pin Setup Time	1.2	-	-	0.6	-	-	μs
$t_{HD.WP}$	WP pin Hold Time	1.2	-	-	0.6	-	-	μs
t_{WR}	Write Cycle Time	-	-	5	-	-	5	ms

Table5

Notes:

1. This parameter is characterized and is not 100% tested.

2. AC measurement conditions:

RL (connects to VCC): 1.3 k (2.5V, 5V), 10 k (1.7V)

Input pulse voltages: 0.3 VCC to 0.7 VCC

Input rise and fall time: 50 ns

Input and output timing reference voltages: 0.5 VCC

The value of RL should be concerned according to the actual loading on the user's system.

Bus Timing

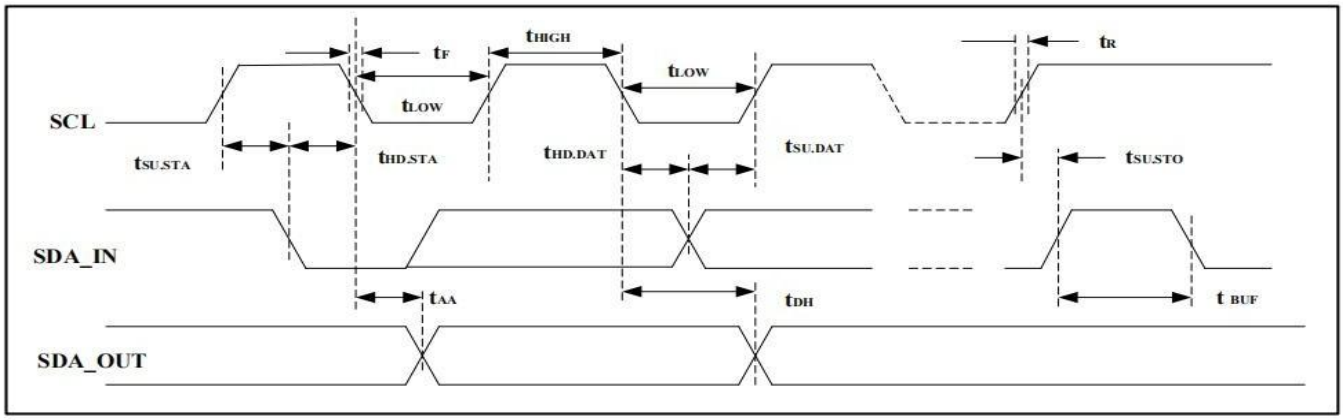


Figure 11. SCL: Serial Clock, SDA: Serial Data I/O

Write Cycle Timing

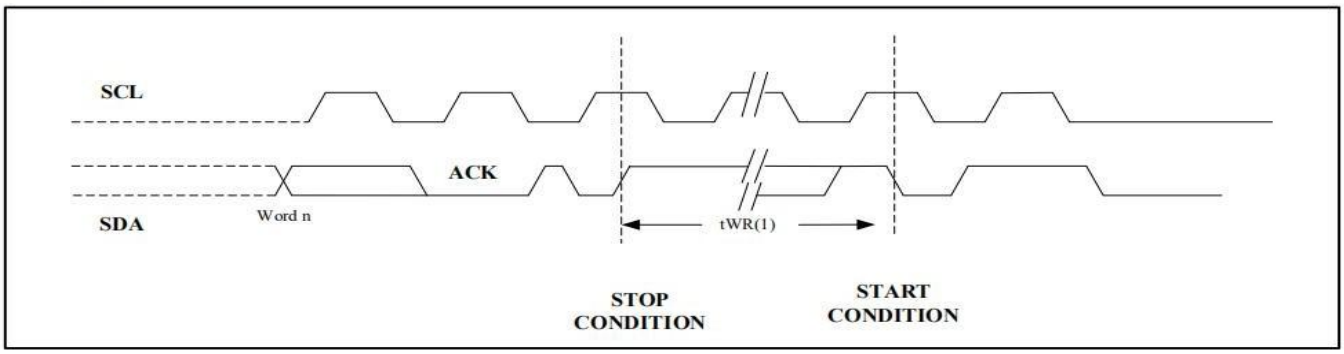


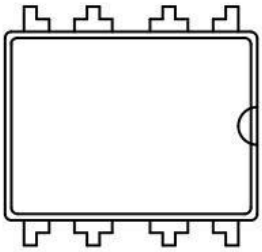
Figure 12. SCL: Serial Clock, SDA: Serial Data I/O

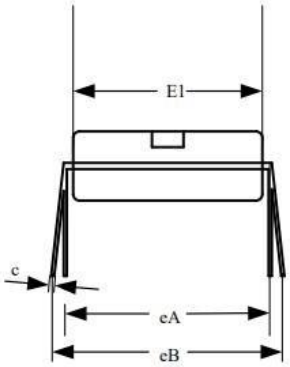
Notes:

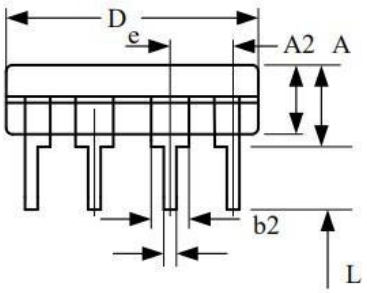
The write cycle time tWR is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

9.Package Information

PDIP Outline Dimensions



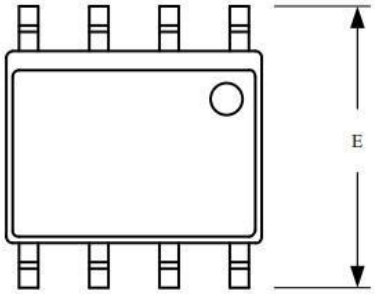


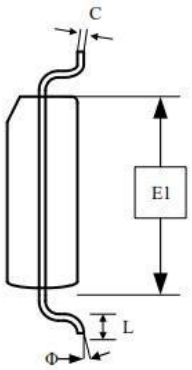


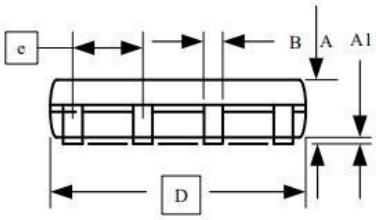
COMMON DIMENSIONS
(Unit of Measure=mm)

SYMBOL	MIN	NOM	MAX
A	3.60	3.80	4.00
A2	3.20	3.30	3.40
b	0.44	-	0.53
b2		1.52BSC	
c	0.24	-	0.32
D	9.05	9.25	9.45
E1	6.15	6.35	6.55
e		2.54BSC	
eA		7.62BSC	
eB	7.62	-	9.30
L		3.00BSC	

SOP



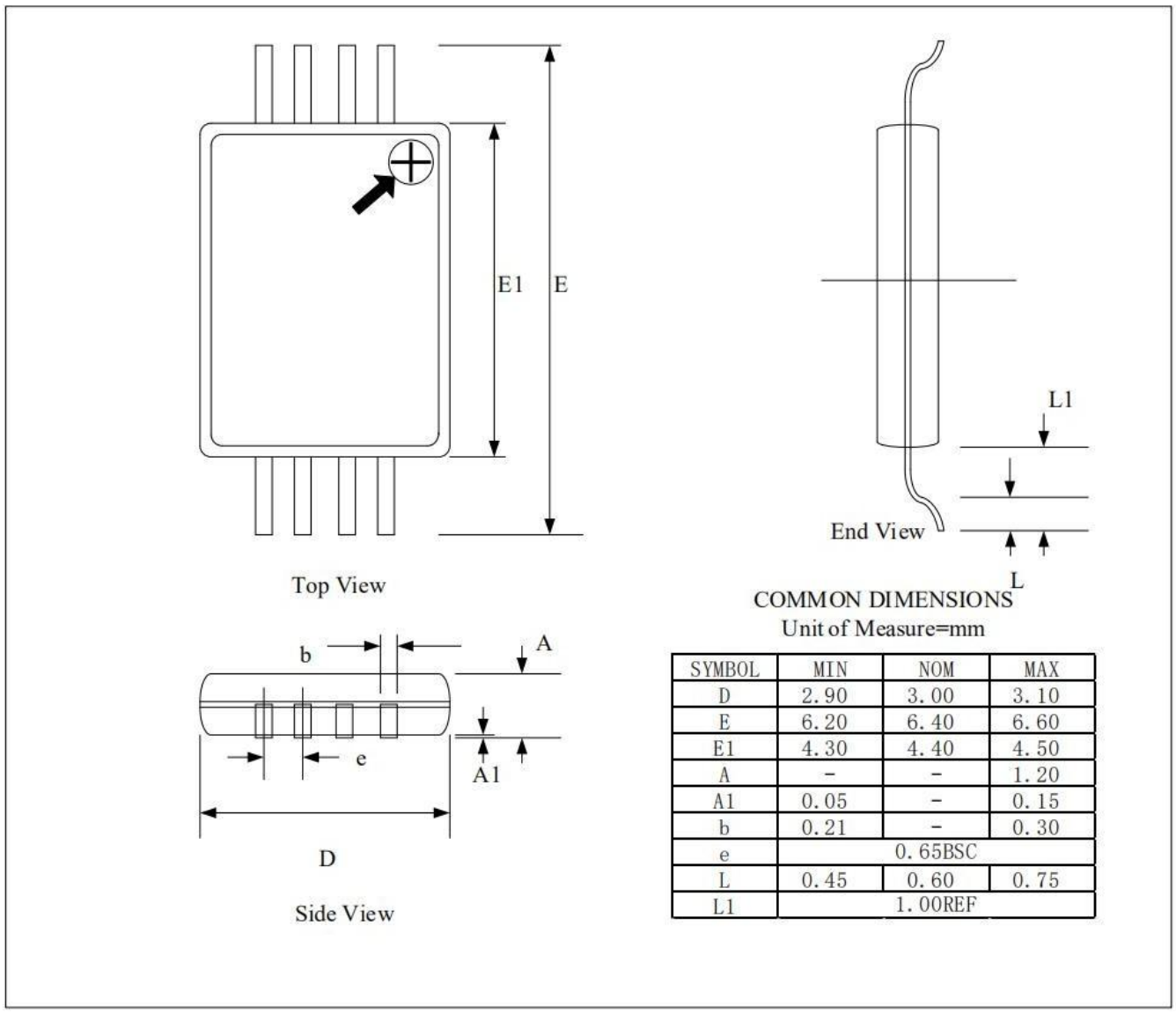




COMMON DIMENSIONS
(Unit of Measure=mm)

SYMBOL	MIN	NOM	MAX
A	1.35	-	1.75
A1	0.10	-	0.23
B	0.39	-	0.48
C	0.21	-	0.26
D	4.70	4.90	5.10
E1	3.70	3.90	4.10
E	5.80	6.00	6.20
e		1.27BSC	
L	0.50	-	0.80
Φ	0°	-	8°

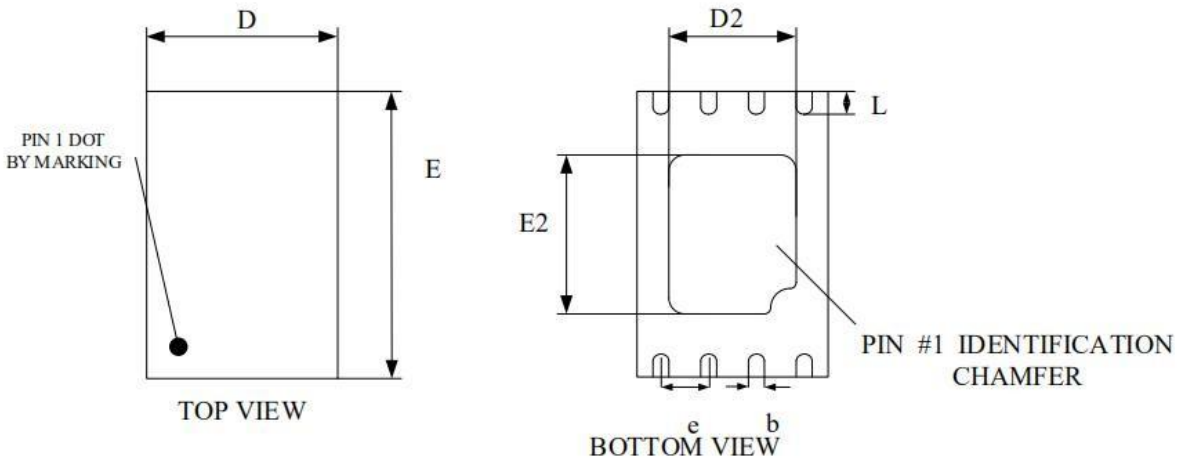
TSSOP



COMMON DIMENSIONS
Unit of Measure=mm

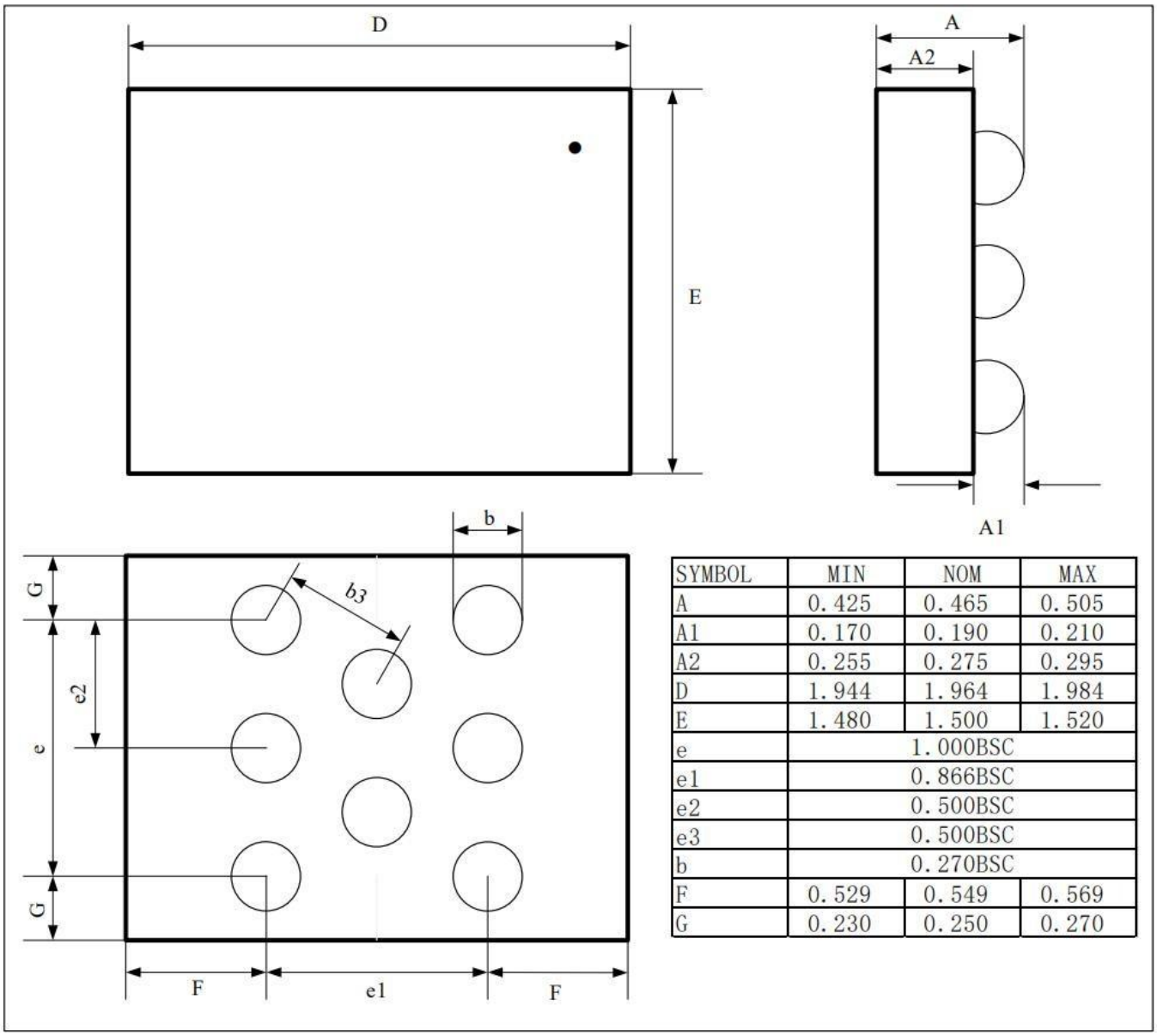
SYMBOL	MIN	NOM	MAX
D	2.90	3.00	3.10
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
A	-	-	1.20
A1	0.05	-	0.15
b	0.21	-	0.30
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00REF		

UDFN



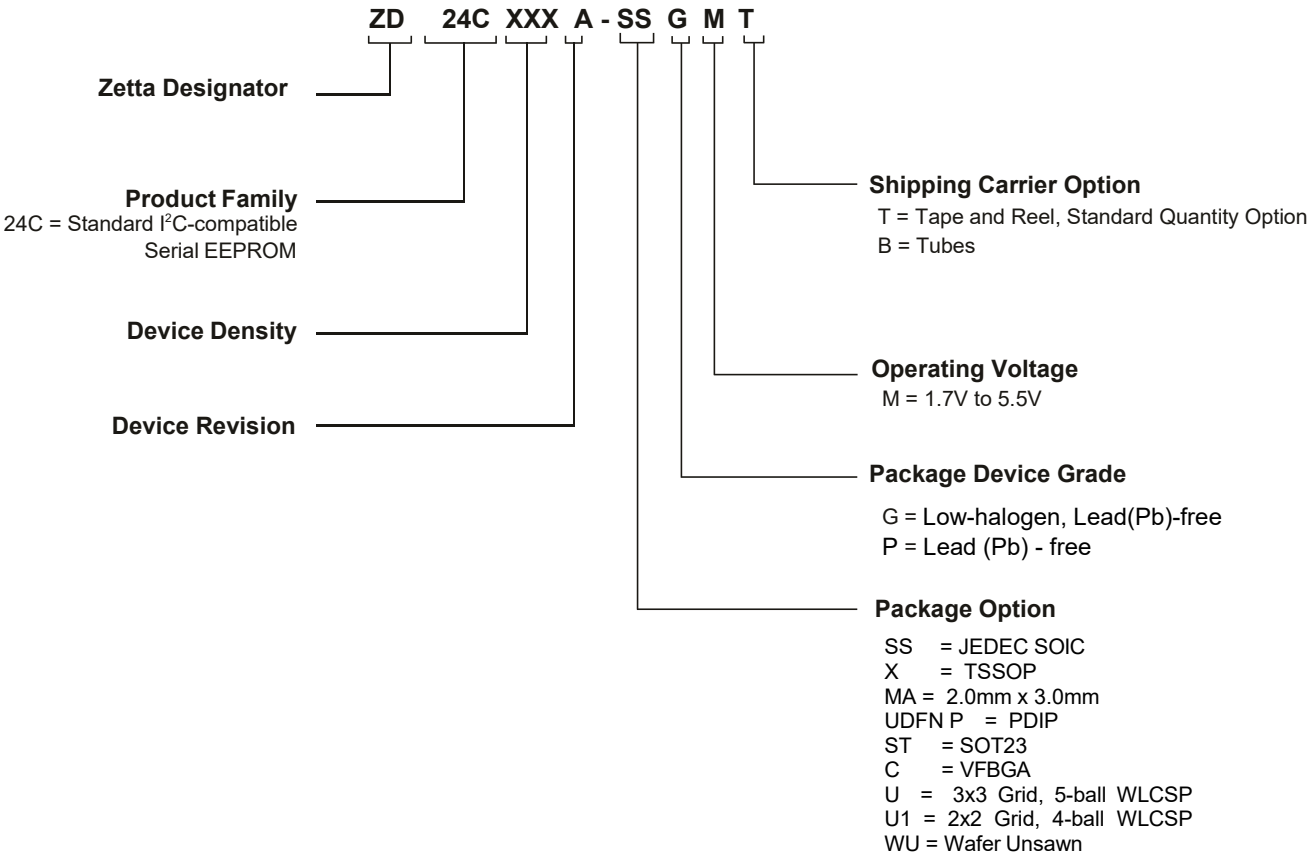
COMMON DIMENSION(MM)			
PKG	UT:ULTRA THIN		
REF	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0.00	-	0.05
A3	0.15REF		
D	1.95	2.00	2.05
E	2.95	3.00	3.05
b	0.20	0.25	0.30
L	0.20	0.30	0.40
D2	1.25	1.40	1.50
E2	1.15	1.30	1.40
e	0.50BSC		

WLCSP



SYMBOL	MIN	NOM	MAX
A	0.425	0.465	0.505
A1	0.170	0.190	0.210
A2	0.255	0.275	0.295
D	1.944	1.964	1.984
E	1.480	1.500	1.520
e	1.000BSC		
e1	0.866BSC		
e2	0.500BSC		
e3	0.500BSC		
b	0.270BSC		
F	0.529	0.549	0.569
G	0.230	0.250	0.270

10.Ordering Information



Revision History

Date	Comments
05/2020	Initial document release.
12/2021	Update package information
11/2022	Update AC/DC table